PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Salman Akram

Patent No.: 7,071,557 B2

Issued: July 4, 2006

For: METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME

Attorney Docket No.: 2269-3442.2US

VIA ELECTRONIC FILING

September 27, 2007

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT OFFICE MISTAKES (37 C.F.R. § 1.322)

Attn.: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

It is noted that several errors appear in this patent of a typographical nature. These errors are due to mistakes in printing on the part of the U.S. Patent and Trademark Office, and occurred through no fault of the Applicant. A certificate of correction in the form attached hereto is requested.

Please note that a Letter to Chief Draftsman was filed concurrently with a Preliminary Amendment on August 1, 2000, a Transmittal of Formal Drawings with Formal Drawings was filed on June 26, 2001, and the Letter to Chief Draftsman filed on August 1, 2000, was again filed with the Patent Office on December 26, 2002 with an Amendment Under 37 C.F.R. § 1.116

(copies enclosed), but annotated informal drawings were used on the printed patent instead of the the clean replacement formal drawings. Attached are copies of the previously filed papers and the date-stamped postcards, acknowledging receipt by the PTO, to provide proof of such filing. We have included subject matter of these papers on the attached PTO/SB/44.

Please send the Certificate to:

Name: Krista Weber Powell
Address: TraskBritt
P.O. Box 2550
Salt Lake City, Utah 84110

Attached hereto is Form PTO/SB/44, which is suitable for printing.

Respectfully submitted,

Krista Weber Powell
Registration No. 47,867
Attorney for Applicant(s)
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: September 27, 2007
KWP/csw

Attachments: PTO/SB/44
Copy of Letter to Chief Draftsman
Copy of Transmittal of Formal Drawings with Formal Drawings
Copy of Amendment Under 37 C.F.R. § 1.116
Copy of date-stamped postcards

Document in ProLaw

PTO/SB/44 (09-07)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,071,557 B2
APPLICATION NO.: 09/388,031
ISSUE DATE : July 4, 2006
INVENTOR(S) : Salman Akram

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page:

Replace the existing annotated figures at the bottom of the page with corrected formal drawings submitted June 26, 2001

In the drawings:

Figure 3a	Replace the existing annotated figure with the corrected formal drawing submitted June 26, 2001
Figure 3b	Replace the existing annotated figure with the corrected formal drawing submitted June 26, 2001
Figure 5	Replace the existing annotated figure with the corrected formal drawing submitted June 26, 2001

In the specification:

COLUMN 7, LINE 52, change "for sec ond" to --for second--

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Krista Weber Powell
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

PTO/SB/44 (09-07)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,071,557 B2
APPLICATION NO.: 09/388,031
ISSUE DATE : July 4, 2006
INVENTOR(S) : Salman Akram

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims:

CLAIM 45, COLUMN 12, LINE 47, change "The structure of claim **41**," to --The structure of claim **44**,--

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Krista Weber Powell
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

PTO/SB/44 (09-07)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

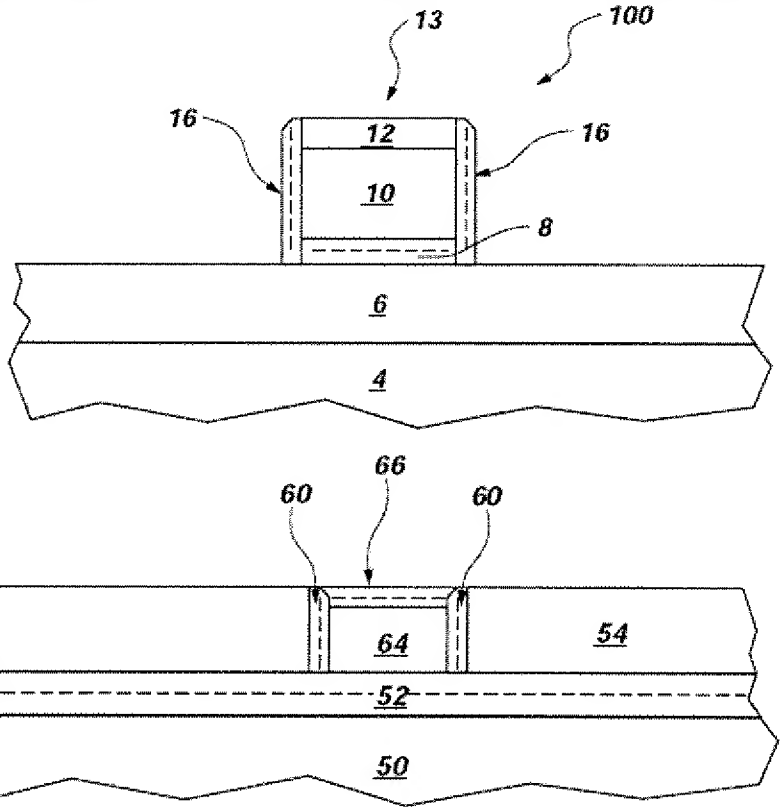
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,071,557 B2
APPLICATION NO.: 09/388,031
ISSUE DATE : July 4, 2006
INVENTOR(S) : Salman Akram

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Please replace the figures appearing on the title page with the following replacement figures:



MAILING ADDRESS OF SENDER (Please do not use customer number below):

Krista Weber Powell
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

PTO/SB/44 (09-07)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,071,557 B2
APPLICATION NO.: 09/388,031
ISSUE DATE : July 4, 2006
INVENTOR(S) : Salman Akram

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Please replace Fig. 3a with the following replacement figure:

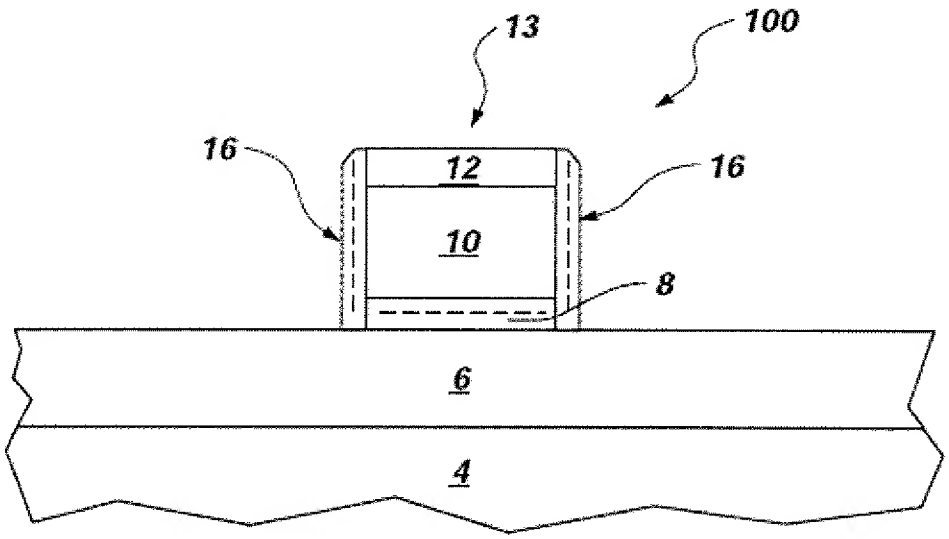


Fig. 3a

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Krista Weber Powell
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

PTO/SB/44 (09-07)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,071,557 B2
APPLICATION NO.: 09/388,031
ISSUE DATE : July 4, 2006
INVENTOR(S) : Salman Akram

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Please replace Fig. 3b with the following replacement figure:

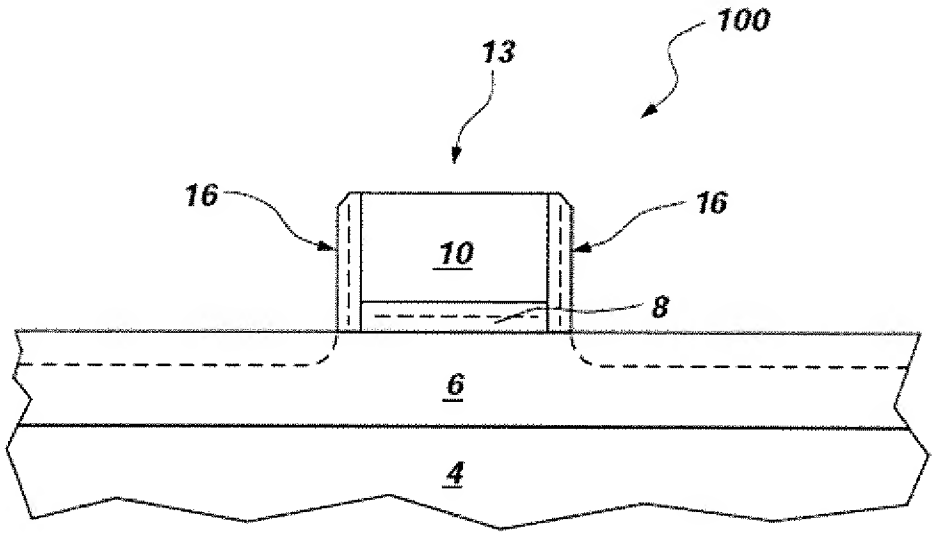


Fig. 3b

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Krista Weber Powell
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

PTO/SB/44 (09-07)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO	:	7,071,557 B2
APPLICATION NO.:		09/388,031
ISSUE DATE	:	July 4, 2006
INVENTOR(S)	:	Salman Akram

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Please replace Fig. 5 with the following replacement figure:

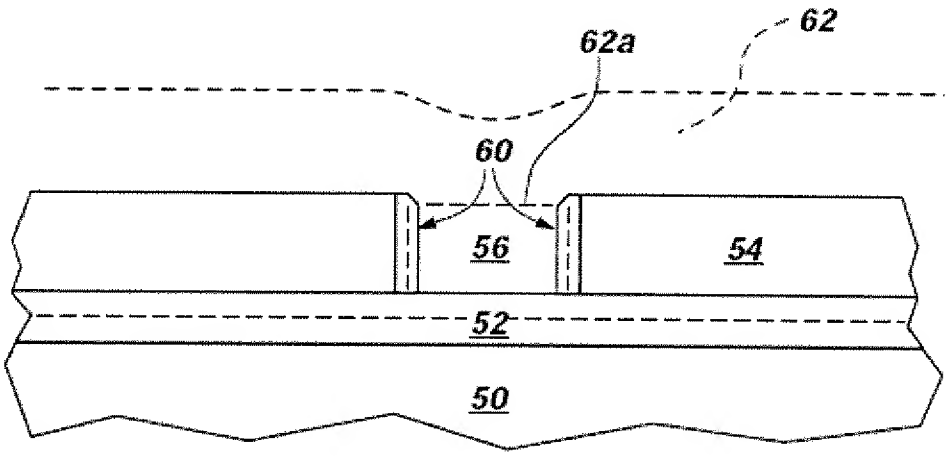
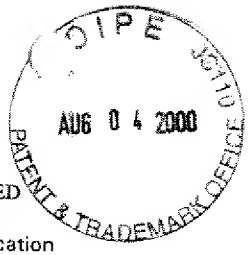


Fig. 5

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Krista Weber Powell
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA



THE PATENT & TRADEMARK OFFICE MAILROOM DATE STAMPED HEREON IS AN ACKNOWLEDGEMENT THAT ON THIS DATE THE PATENT & TRADEMARK OFFICE RECEIVED: Utility Patent Application

Preliminary Amendment (4 pages); Letter to the Chief Draftsman (2 pages) and attached revised figures with annotations in red (3 sheets, 3 figures).

Invention: METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME
Applicant(s): Salman Akram
Filing Date: September 1, 1999
Serial No.: 09/388,031
Date Sent: August 1, 2000 via First Class Mail
Client/Matter Docket No.: 2269/3442US JAW/dlm

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Salman Akram

Serial No.: 09/388,031

Filed: September 1, 1999

For: METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME

Examiner: To be assigned

Group Art Unit: 2812

Attorney Docket No.: 3442US (96-428)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail (under 37 C.F.R. § 1.8(a)) on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, Washington, D.C. 20231.

August 1, 2000
Date of Deposit

Signature of registered practitioner or other person having reasonable basis to expect mailing to occur on date of deposit shown pursuant to 37 C.F.R. § 1.8(a)(1)(ii)

Joseph A. Walkowski
Typed/printed name of person whose signature is contained above

LETTER TO THE CHIEF DRAFTSMAN

Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicant submits herewith revised FIGS. 3a, 3b and 5 which correct errors in the drawings. Specifically, FIGS. 3a and 3b have been revised to add the reference numeral 100 with appropriate lead lines; and FIG. 5 has been revised to add the reference numeral 62a.

No new matter has been added. Approval of the proposed revisions is respectfully requested.

Respectfully submitted,

Joseph A. Walkowski
Registration No. 28,765
Attorney for Applicant
TRASK BRITT
P. O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: (801) 532-1922

Date: August 1, 2000

JAW/kf:dlm

N:\2269\3442\Letter to Chief Draftsman.wpd

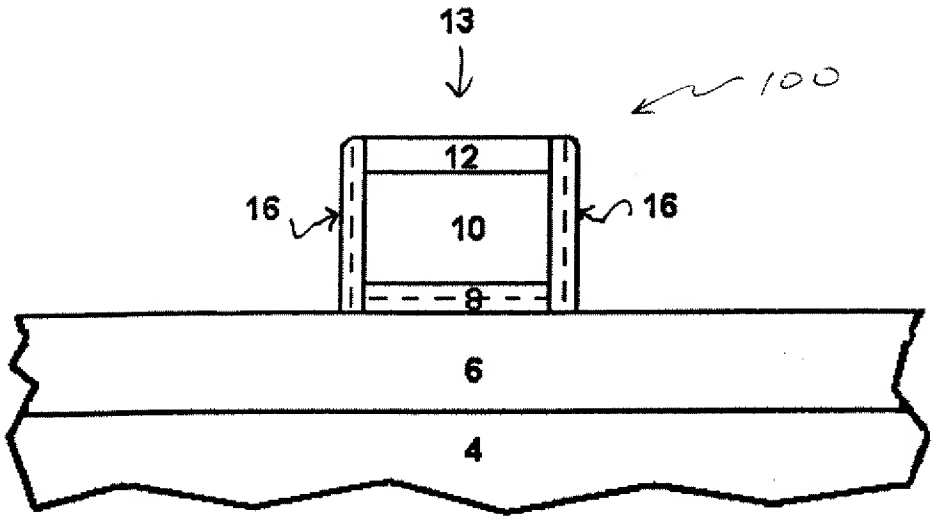


Figure 3a

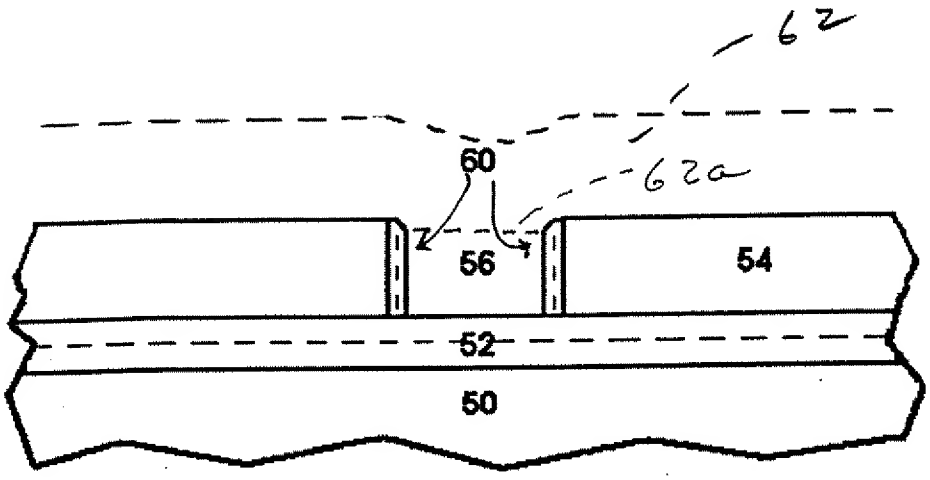


Figure 5

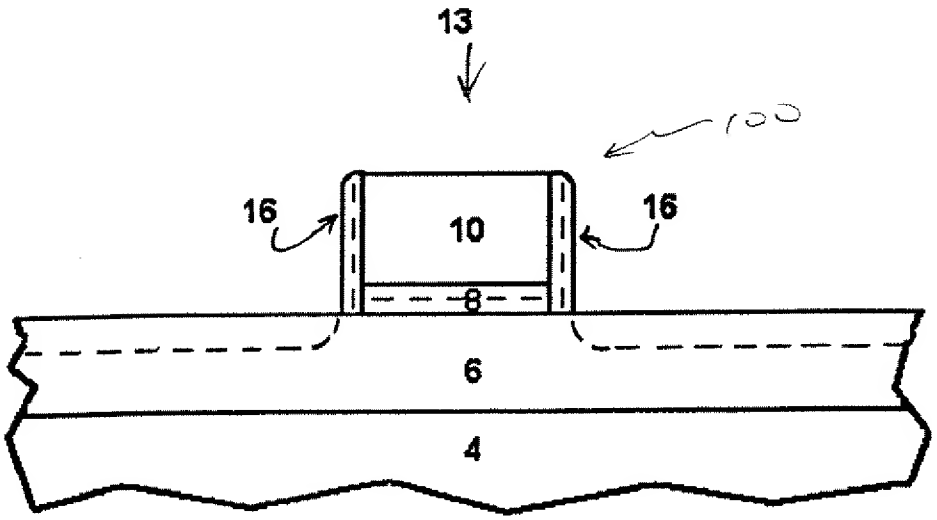


Figure 3b

THE PATENT & TRADEMARK OFFICE MAILROOM DATE STAMPED HEREON IS AN ACKNOWLEDGEMENT THAT ON THIS DATE THE PATENT & TRADEMARK OFFICE RECEIVED:

Transmittal of Formal Drawings with Formal Drawings (7 pages 14 Total FIGS).

Invention: METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME
Applicant(s): Salman Akram
Filing Date: September 1, 1999
Serial No.: 09/388,031
Date Sent: June 26, 2001 via First Class Mail
Client/Matter Docket No.: 2269/3442US (96-388)
KWP/dh

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Salman Akram

Serial No.: 09/388,031

Filed: September 1, 1999

For: METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME

Examiner: W. Lindsay, Jr.

Group Art Unit: 2812

Attorney Docket No.: 3442US (96-428)

CERTIFICATE OF MAILING

I hereby certify that this paper or fee along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail (under 37 C.F.R. § 1.8(a)) on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, Washington, D.C. 20231.

June 26, 2001
Date of Deposit

Darlene Holt
Signature of registered practitioner or other person having reasonable basis to expect mailing to occur on date of deposit shown pursuant to 37 C.F.R. § 1.8(a)(1)(ii)

Darlene Holt
Typed/printed name of person whose signature is contained above

TRANSMITTAL OF FORMAL DRAWINGS

Commissioner for Patents
Washington, D.C. 20231

Sir:

Attached please find the formal drawings for this application.

Respectfully submitted,

Krista Weber Powell
Registration No. 47,867
Attorney for Applicant
TRASKBRITT, PC
P. O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: (801) 532-1922

Date: June 26, 2001
KWP/dh

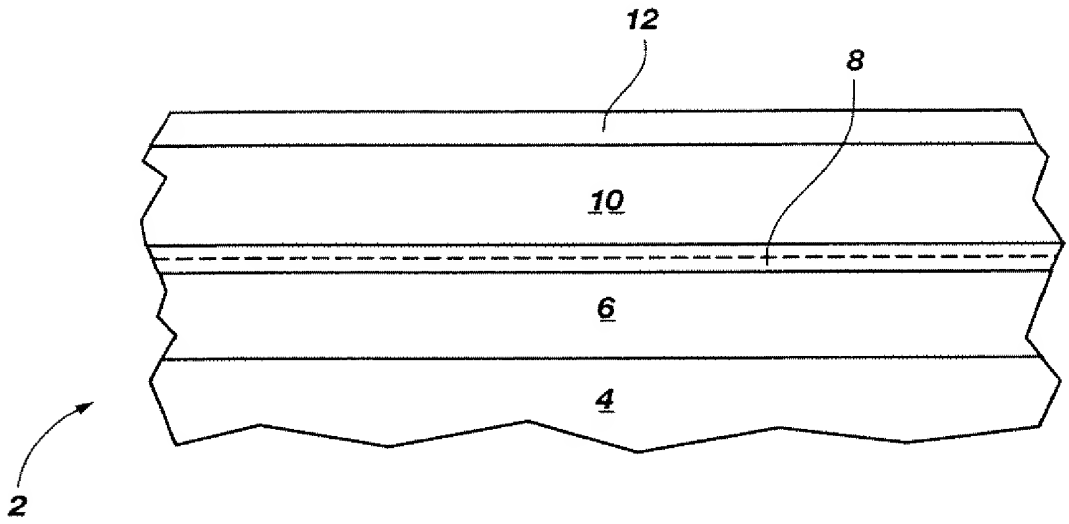


Fig. 1

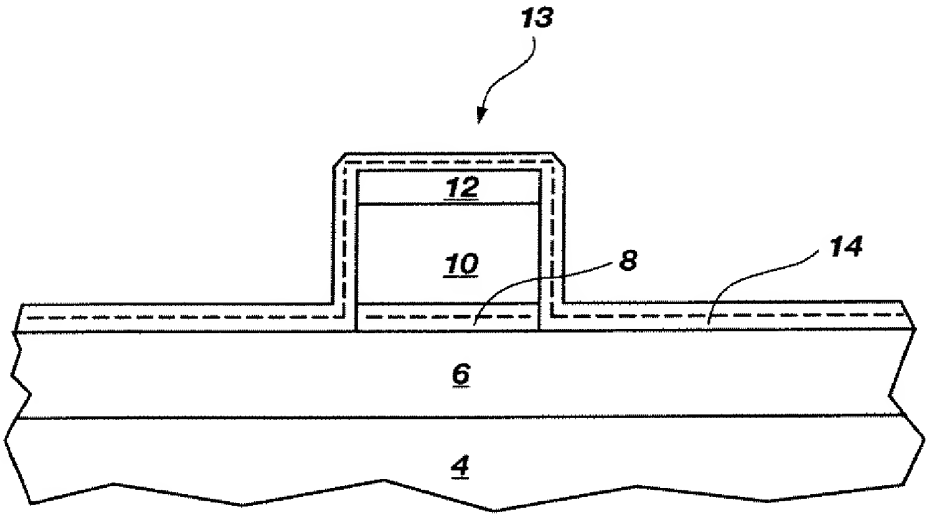


Fig. 2

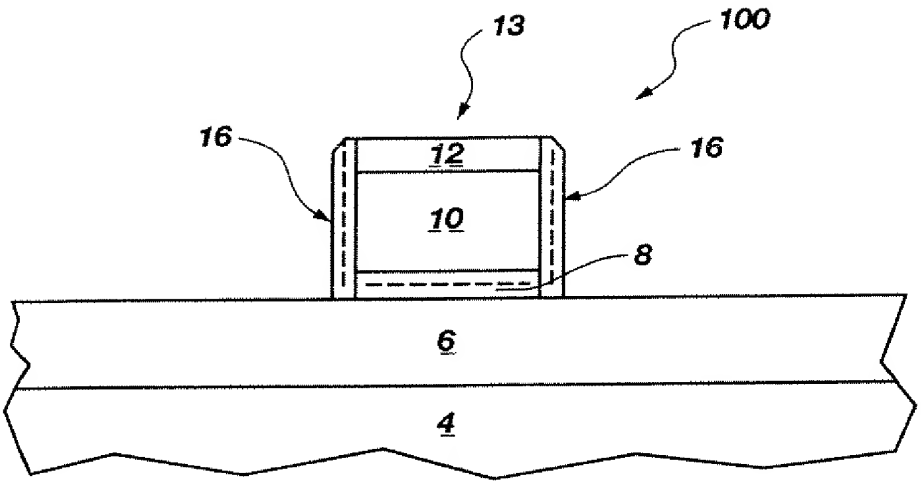


Fig. 3a

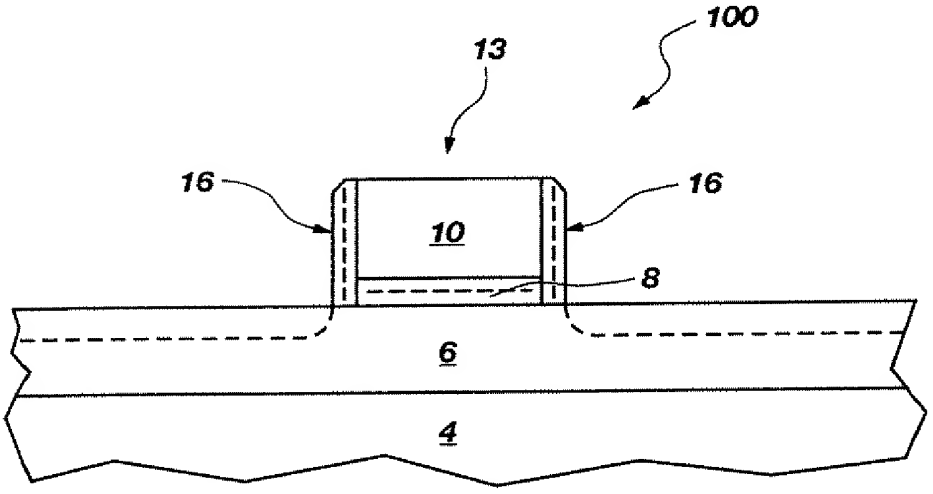


Fig. 3b

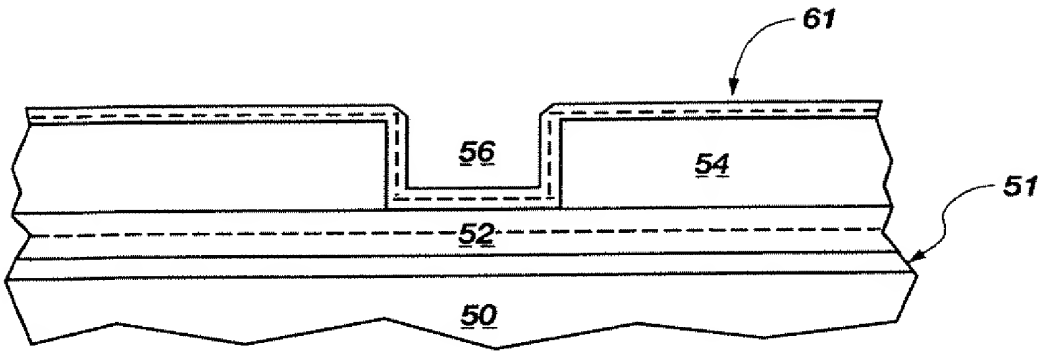


Fig. 4

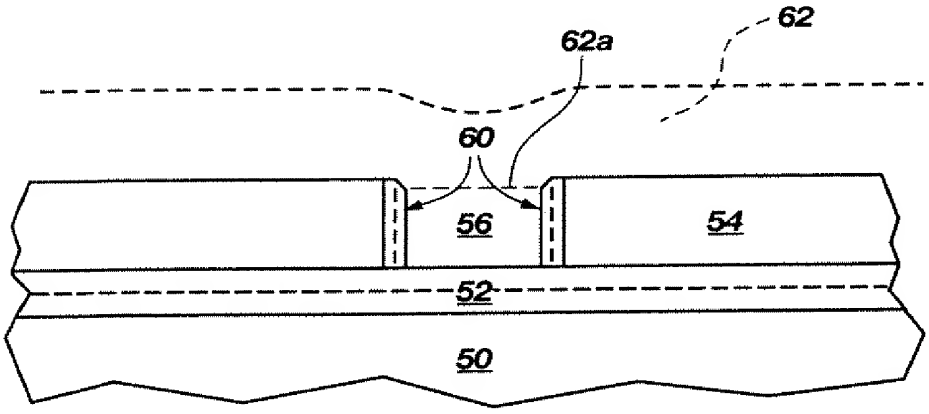


Fig. 5

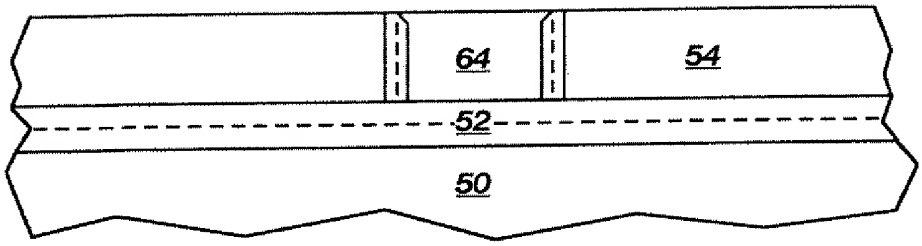


Fig. 6

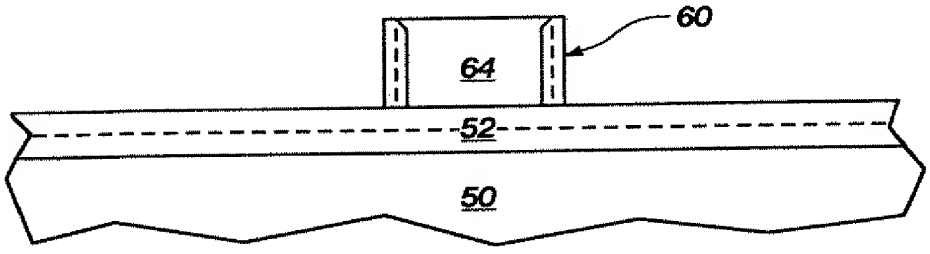


Fig. 7a

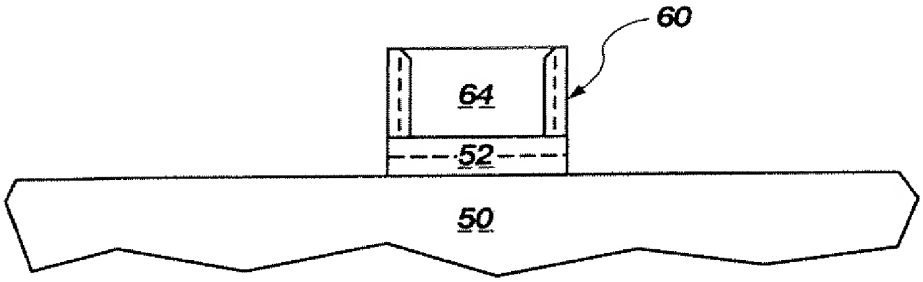


Fig. 7b

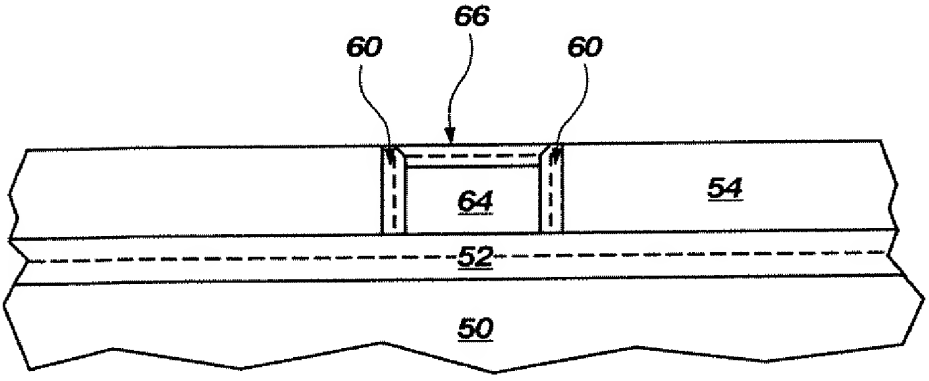


Fig. 8

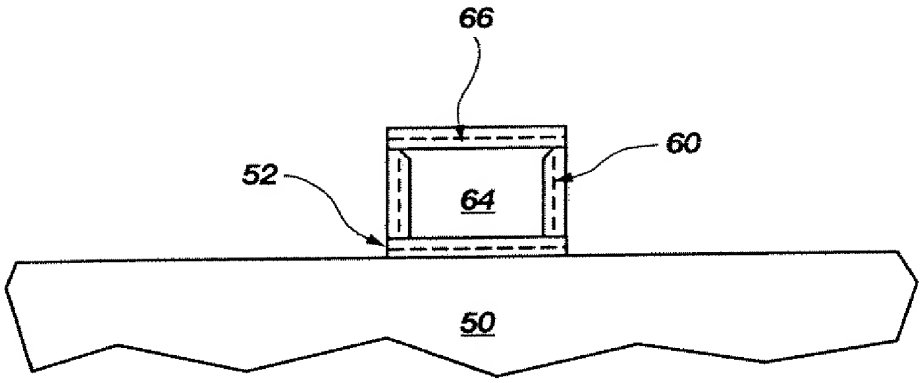


Fig. 9

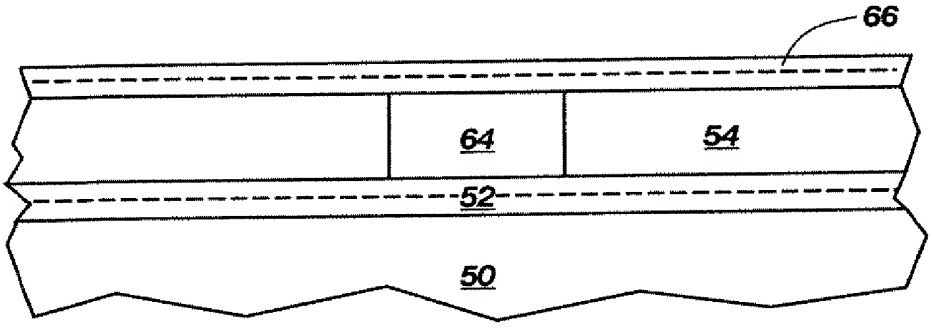


Fig. 10

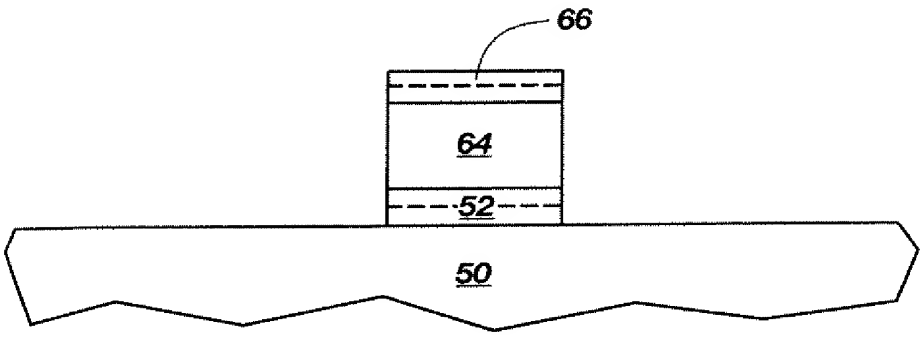


Fig. 11

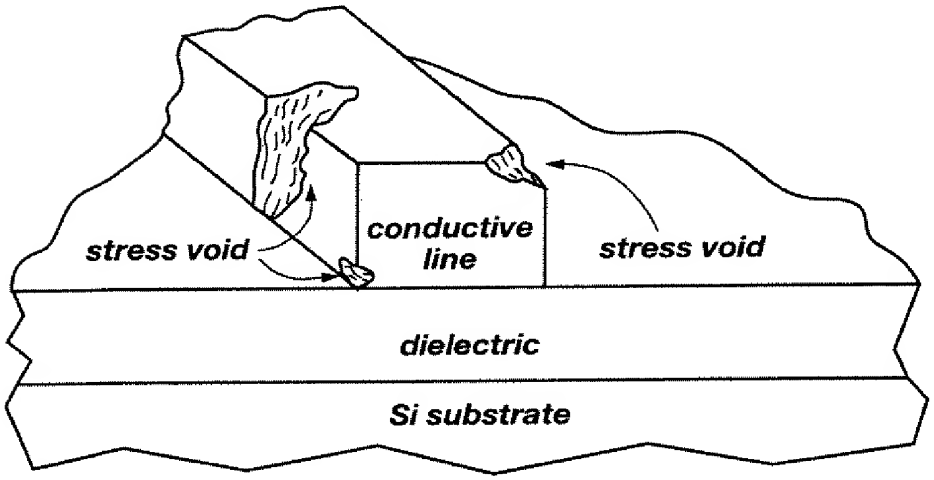


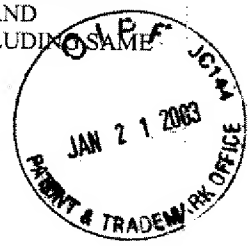
Fig. 12
(PRIOR ART)

FR

TH ATENT & TRADEMARK OFFICE MAILROOM TE
ST PED HEREON IS AN ACKNOWLEDGEMENT T T ON THIS
DATE THE PATENT & TRADEMARK OFFICE RECEIVED:

Transmittal Form (in duplicate); Amendment under 37 C.F.R. § 1.116 in response to final office action dated September 25, 2002; USPTO date stamped postcard; Letter to Chief Draftsman and FIGS. 3a, 3b previously filed on August 4, 2000.

Invention:	METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME
Applicant(s):	Salman Akram
Filing Date:	September 1, 1999
Serial No.:	09/388,031
Date Sent:	December 26, 2002 via first class mail
Docket No.:	2269-3442.2US
JAW/dp:lb	



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Salman Akram

Serial No.: 09/388,031

Filed: September 1, 19999

For: METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME

Confirmation No.: 3303

Examiner: E. Lee

Group Art Unit: 2815

Attorney Docket No.: 3442.2US (96-428)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail (under 37 C.F.R. § 1.8(a)) on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, Washington, D.C. 20231.

December 26, 2002
Date of Deposit

Signature of registered practitioner or other person having reasonable basis to expect mailing to occur on date of deposit shown pursuant to 37 C.F.R. § 1.8(a)(1)(ii)

Joseph A. Walkowski
Typed/printed name of person whose signature is contained above

AMENDMENT UNDER 37 C.F.R. §1.116

Box AF
Commissioner for Patents
Washington, D.C. 20231

Sir:

The following amendments and remarks are filed in response to the Examiner's remarks in the Final Office Action mailed September 25, 2002, the three-month shortened statutory period for response to which expires on December 25, 2002. This response is submitted on or before three months from the mailing date of the Final Office Action, December 25, 2002 being a holiday.

IN THE CLAIMS:

Please note that all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity.

Please amend the claims as follows:

1. (Four times amended) A metallization structure for a semiconductor device, comprising:

a substrate comprising a substantially planar upper surface; and

a conductive line for transmitting a signal laterally across said substrate, said conductive line comprising:

a metal layer defining a pattern on a portion of the substrate upper surface;

a single conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said single conducting layer having substantially aligned sidewalls and said single conducting layer including an upper surface out of contact with any metal and defining an upper surface of said conductive line; and

metal spacers flanking and extending at least substantially to a height of the sidewalls of the single conducting layer and metal layer.

2. (Reiterated) The metallization structure of claim 1, further comprising a dielectric layer on the substrate upper surface and underlying the metal layer.

3. (Reiterated) The metallization structure of claim 2, wherein the dielectric layer is silicon oxide or BPSG.

4. (Reiterated) The metallization structure of claim 1, wherein the metal layer is a first metal layer comprising Ti, Ta, W, Co or Mo or alloys or compounds thereof, including TaN or TiN.

5. (Reiterated) The metallization structure of claim 4, further including a second metal layer disposed between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

6. (Reiterated) The metallization structure of claim 5, wherein the first metal layer comprises titanium or titanium nitride.

7. (Reiterated) The metallization structure of claim 1, wherein the metal layer is titanium or titanium nitride.

8. (Previously amended) The metallization structure of claim 1, wherein the single conducting layer is selected from the group comprising aluminum and copper.

9. (Previously amended) The metallization structure of claim 8, wherein the single conducting layer is an aluminum-copper alloy.

10. (Reiterated) The metallization structure of claim 1, wherein the metal spacers comprise at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

11. (Previously twice amended) The metallization structure of claim 1, wherein the metal spacers are titanium or titanium nitride.

12. (Three times amended) The metallization structure of claim 1, further comprising a dielectric layer on the single conducting layer and having sidewalls aligned with said sidewalls of the single conducting layer, the metal spacers extending along the sidewalls of the dielectric layer.

13. (Reiterated) The metallization structure of claim 12, wherein the dielectric layer comprises a low dielectric constant material.

14. (Reiterated) The metallization structure of claim 13, wherein the dielectric layer is fluorine-doped silicon oxide.

15. (Reiterated) The metallization structure of claim 1, wherein the metal layer and the metal spacers comprise the same metal.

16. (Four times amended) A metallization structure for a semiconductor device, comprising:

a substrate having a metal layer extending over said substrate, said metal layer at least underlying a conductive line, said conductive line for transmitting a signal across said substrate;

a dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said at least one sidewall of said aperture defining said conductive line;

a metal spacer abutting at least one sidewall of said at least one sidewall of the aperture and in contact with said dielectric layer, said metal spacer in contact with said underlying metal layer; and

a conductive layer in contact with said metal spacer, said conductive layer substantially filling a remaining portion of the aperture and having an upper surface substantially coincident with an upper surface of said dielectric layer.

17. (Reiterated) The metallization structure of claim 16, wherein the metal layer comprises tantalum, titanium, tungsten, cobalt, molybdenum, or an alloy or a compound of any thereof, including TaN and TiN.

18. (Reiterated) The metallization structure of claim 17, wherein the metal layer is titanium or titanium nitride.

19. (Previously amended) The metallization structure of claim 16, wherein the metal spacer includes at least one layer of metal comprising tantalum, titanium, tungsten, cobalt, molybdenum, or alloys or compounds thereof, including TaN and TiN.

20. (Previously amended) The metallization structure of claim 19, wherein the metal spacer is titanium or titanium nitride.

21. (Reiterated) The metallization structure of claim 16, wherein the substrate comprises a dielectric layer underlying the metal layer.

22. (Reiterated) The metallization structure of claim 21, wherein the dielectric layer underlying the metal layer is silicon oxide or BPSG.

23. (Amended twice) The metallization structure of claim 16, wherein the metal layer and the metal spacer comprise the same metal.

24. (Reiterated) The metallization structure of claim 16, wherein the metal layer is a first metal layer comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

25. (Reiterated) The metallization structure of claim 24, further including a second metal layer disposed between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

26. (Amended) A metallization structure for a semiconductor device, comprising:

a substrate having a metal layer extending over said substrate, said metal layer at least underlying a conductive line, said conductive line for transmitting a signal across said substrate;

a dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said at least one sidewall of said aperture defining said conductive line;

a metal spacer abutting at least one sidewall of said at least one sidewall of the aperture and in contact with said dielectric layer, said metal spacer in contact with said underlying metal layer;

a conductive layer in contact with said metal spacer, said conductive layer substantially filling a remaining portion of the aperture; and

at least one upper metal layer on the conductive layer comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN, said at least one upper metal layer being disposed within said aperture laterally adjacent said metal spacer and having an upper surface substantially coincident with an upper surface of said dielectric layer and an uppermost extent of said metal spacer.

27. (Reiterated) The metallization structure of claim 26, wherein the at least one upper metal layer comprises a plurality of upper metal layers.

28. (Previously amended) The metallization structure of claim 26, wherein the at least one upper metal layer comprises titanium or titanium nitride.

100. (Reiterated) The metallization structure of claim 2, wherein said dielectric layer extends completely underneath said conductive line.

101. (Reiterated) The metallization structure of claim 16, wherein said aperture contains conductive material.

102. (Three times amended) A structure for transmitting a signal across a semiconductor device, said structure comprising:

a substrate comprising a substantially planar upper surface; and

a conductive line extending over said upper surface and isolated therefrom by a dielectric layer at least underlying said conductive line, said conductive line comprising:

a metal layer above said dielectric layer, said metal layer defining a pattern on a portion of the substrate upper surface;

a single conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said single conducting layer having substantially aligned sidewalls, wherein an upper surface of said single conductive layer is out of contact with any metal and defines an upper surface of said conductive line; and

metal spacers flanking and extending at least substantially to a height of the sidewalls of the single conducting layer and metal layer

103. (Reiterated) The structure of claim 102, wherein the dielectric layer is silicon oxide or BPSG.

104. (Reiterated) The structure of claim 102, wherein the metal layer is a first metal layer comprising Ti, Ta, W, Co or Mo or alloys or compounds thereof, including TaN or TiN.

105. (Reiterated) The structure of claim 104, further including a second metal layer disposed between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

106. (Reiterated) The structure of claim 105, wherein the first metal layer comprises titanium or titanium nitride.

107. (Reiterated) The structure of claim 102, wherein the metal layer is titanium or titanium nitride.

108. (Previously amended) The structure of claim 102, wherein the single conducting layer is selected from the group comprising aluminum and copper.

109. (Previously amended) The structure of claim 108, wherein the single conducting layer is an aluminum-copper alloy.

110. (Reiterated) The structure of claim 102, wherein the metal spacers comprise at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

111. (Reiterated) The structure of claim 102, wherein the metal spacers are titanium or titanium nitride.

112. (Previously amended) The structure of claim 102, further comprising a dielectric layer on the single conducting layer and having sidewalls aligned with said sidewalls of the single conducting layer, the metal spacers extending along the sidewalls of the dielectric layer.

113. (Reiterated) The structure of claim 112, wherein the dielectric layer comprises a low dielectric constant material.

114. (Reiterated) The structure of claim 113, wherein the dielectric layer is fluorine-doped silicon oxide.

115. (Reiterated) The structure of claim 102, wherein the metal layer and the metal spacers comprise the same metal.

116. (Three time amended) A structure for transmitting a signal laterally across a substrate of a semiconductor device, said structure comprising:

a substrate having a metal layer of a conductive line disposed thereon;

a dielectric layer above said metal layer, said dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said aperture at least extending a length of said conductive line;

a metal spacer flanking at least one sidewall of said at least one sidewall of the aperture and in contact with said dielectric layer, said metal spacer in contact with said underlying metal layer; and

a conductive layer in contact with said metal spacer, said conductive layer substantially filling a remaining portion of the aperture and having an upper surface substantially coincident with an upper surface of said dielectric layer.

117. (Reiterated) The structure of claim 116, wherein the metal layer comprises tantalum, titanium, tungsten, cobalt, molybdenum, or an alloy or a compound of any thereof, including TaN and TiN.

118. (Reiterated) The structure of claim 117, wherein the metal layer is titanium or titanium nitride.

119. (Reiterated) The structure of claim 116, wherein the metal spacer includes at least one layer of metal comprising tantalum, titanium, tungsten, cobalt, molybdenum, or alloys or compounds thereof, including TaN and TiN.

120. (Reiterated) The structure of claim 119, wherein the metal spacer is titanium or titanium nitride.

121. (Reiterated) The structure of claim 116, wherein the substrate comprises a dielectric layer underlying the metal layer.

122. (Reiterated) The structure of claim 121, wherein the dielectric layer underlying the metal layer is silicon oxide or BPSG.

123. (Reiterated) The structure of claim 116, wherein the metal layer and the metal spacer comprise the same metal.

124. (Reiterated) The structure of claim 116, wherein the metal layer is a first metal layer comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

125. (Reiterated) The structure of claim 124, further including a second metal layer disposed between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

126. (Amended) A structure for transmitting a signal laterally across a substrate of a semiconductor device, said structure comprising:

a substrate having a metal layer of a conductive line disposed thereon;

a dielectric layer above said metal layer, said dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said aperture at least extending a length of said conductive line;

a metal spacer flanking at least one sidewall of said at least one sidewall of the aperture and in contact with said dielectric layer, said metal spacer in contact with said underlying metal layer;

a conductive layer in contact with said metal spacer, said conductive layer substantially filling a remaining portion of the aperture; and

at least one upper metal layer on the conductive layer and comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN, said at least one upper metal layer being disposed within said aperture laterally adjacent said metal spacer and having an upper surface substantially coincident with an upper surface of said dielectric layer and an uppermost extent of said metal spacer.

127. (Reiterated) The structure of claim 126, wherein the at least one upper metal layer comprises a plurality of upper metal layers.

128. (Reiterated) The structure of claim 126, wherein the at least one upper metal layer comprises titanium or titanium nitride.

129. (Reiterated) The structure of claim 116, wherein said metal spacer extends substantially a height of said at least one sidewall.

REMARKS

The Final Office Action mailed September 25, 2002, has been received and reviewed. Claims 1 through 28 and 100 through 129 are currently pending in the application. Claims 1 through 28 and 100 through 129 stand rejected. Applicant proposes to amend claims 1, 12, 16, 26, 102, 116 and 126, and respectfully request reconsideration of the application as proposed to be amended herein.

35 U.S.C. § 112 Claim Rejections

Claims 12 and 112 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant proposes to amend claims 1 and 102 to overcome this rejection.

35 U.S.C. § 102 Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,534,463 to Lee et al.

Claims 16 through 20, 23 through 25, 101, 116 through 120, 123 through 125, and 129 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Lee et al. (U.S. Patent No. 5,534,463). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicant proposes to amend claims 16 and 116 to recite that the metal spacer is in contact with the dielectric layer, and that an upper surface of the conductive layer is substantially coincident with an upper surface of the dielectric layer. Lee fails to teach either of these two limitations. Therefore, claims 16 and 116 are not anticipated. Claims 17 through 20, 23 through

25, 101, 117 through 120, 123 through 125 and 129 are allowable as respectively depending from one of claims 16 and 116.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,074,943 to Brennan et al. in view of U.S. Patent No. 6,277,745 B1 to Liu et al.

Claims 1, 4 through 13, and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Brennan et al. (U.S. Patent No. 6,074,943) in view of Liu et al. (U.S. Patent No. 6,277,745 B1). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Claim 1 as proposed to be amended is allowable over the combination of references, as Brennan et al. and Liu et al., in combination, fail to teach the claimed structure including a single conductive layer "including an upper surface out of contact with any metal and defining an upper surface of said conductive line" (emphasis added). It is noted that Brennan et al. (FIG. 3), relied upon by the Examiner, teaches a single layer interconnect 310 on an unspecified underlying layer 300. Other embodiments of Brennan et al. teach the use of an optional underlying barrier and adhesion layer 205 under interconnect material 210 and of an anti-reflective coating layer 215 thereover. Liu et al. uniformly teaches the use of a conductive copper layer 6 having overlying and underlying metal barrier layers 8 and 4, respectively. There is no teaching, in Brennan et al. and Liu et al. as applied, of a conductive line comprising a metal layer having a single conductive

layer thereover, wherein an upper surface of the single conductive layer is out of contact with any metal and defines an upper surface of the conductive line. Moreover, there is no motivation to combine Liu et al. with Brennan et al. other than the Office's presumption that it would have been obvious to include the bottom barrier layer of Brennan et al. (*sic*- presumably meaning Liu et al.), to passivate the bottom surface of the interconnect of Brennan et al. However, there is no suggestion or motivation provided as to why the combination would be necessary or desirable. It is noted that Brennan also discloses the use of top and bottom metal-containing layers respectively above and below a metal alloy interconnect layer, but not the structure claimed by Applicant of a metal layer having a single conductive layer thereover, the single conductive layer having an upper surface defining an upper surface of a conductive line. Accordingly, the rejection of claim 1 should be withdrawn.

Claims 4 through 13 and 15 depend from claim 1 and, therefore, are allowable. In addition, claim 12 recites the presence of a dielectric layer *on* the single conductive layer, which structure is untaught by the combination of references as applied.

Accordingly, claims 1, 4 through 13 and 15 are allowable.

Obviousness Rejection Based on U.S. Patent No. 6,074,943 to Brennan et al. in view of U.S. Patent No. 6,277,745 B1 to Liu et al., and further in view of U.S. Patent No. 6,166,439 to Cox

Claims 2, 3, 100, 102 through 113, and 115 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Brennan et al. (U.S. Patent No. 6,074,943) in view of Liu et al. (U.S. Patent No. 6,277,745 B1) as applied to claims 1, 4 through 13, and 15 above, and further in view Cox (U.S. Patent No. 6,166,439). Applicant respectfully traverses this rejection, as hereinafter set forth.

As to claims 2, 3 and 100, Cox fails to cure the deficiencies in the teachings of Brennan et al. and Liu et al., as previously discussed above with respect to claim 1, the previous remarks being incorporated herein by reference. As to claims 102 through 113 and 115, Applicant proposes to amend claim 102 in a manner similar to claim 1 (in addition to the amendment to

overcome the 35 U.S.C. 112, second paragraph rejection). Therefore, claim 102 and, consequently, claims 103 through 113 and 115, are allowable for the same reasons as previously set forth with respect to claim 1.

Obviousness Rejection Based on U.S. Patent No. 6,074,943 to Brennan et al. in view of U.S. Patent No. 6,277,745 B1 to Liu et al., and further in view of U.S. Patent No. 6,046,502 to Matsuno

Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Brennan et al. (U.S. Patent No. 6,074,943) in view of Liu et al. (U.S. Patent No. 6,277,745 B1) as applied to claims 1, 4 through 13, and 15 above, and further in view Matsuno (U.S. Patent No. 6,046,502). Applicant respectfully traverses this rejection, as hereinafter set forth.

Claim 14 depends from claim 1. Matsuno fails to cure the previously noted deficiencies in Brennan et al. and Liu et al. Therefore, claim 14 is allowable as depending from claim 1.

Obviousness Rejection Based on U.S. Patent No. 5,534,463 to Lee et al. in view of U.S. Patent No. 6,197,682 B1 to Drynan

Claims 26 through 28 and 126 through 128 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee et al. (U.S. Patent No. 5,534,463) as applied to claims 16 through 20, 23 through 25, 101, 116 through 120, 123 through 125, and 129 above, and further in view of Drynan (U.S. Patent No. 6,197,682 B1). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant proposes to amend claim 26 to place same in independent form, to include the limitations of claim 16 prior to the amendment proposed herein and to add the further limitation that the at least one upper metal layer is disposed within the aperture laterally adjacent the metal spacer and has an upper surface substantially coincident with an upper surface of the dielectric layer and an uppermost extent of the metal spacer (emphasis added). The upper metal layer of Drynan extends above the aperture in the dielectric layer which is laterally adjacent the

metallization structure and, further, projects above the spacers of the Drynan structure. The conductive Lee structure also has an upper surface which projects substantially above the dielectric layer. It is further noted that the Drynan upper metal layer apparently comprises a discrete wiring layer, while Applicant's claimed metallization structure includes the at least one upper metal layer as a part of the structure itself. With references to Applicant's drawing Fig. 8, by way of example only, it is readily apparent that Applicant's conductive layer 64 is flanked by metal spacers 60 and capped by an upper metal layer 66, forming a clad conductive structure defining a conductive line. The Dryman structures, in contrast, comprise discrete wiring layers connected by a vertically extending conductive plug. Accordingly, claims 26 through 28 are allowable.

Applicant proposes to amend claim 126 in a manner substantially the same as claim 26. Claims 126 through 128 are, accordingly, allowable for the same reasons as claims 26 through 28.

Obviousness Rejection Based on U.S. Patent No. 5,534,463 to Lee et al. in view of U.S. Patent No. 6,166,439 to Cox

Claims 21, 22, 121, and 122 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee et al. (U.S. Patent No. 5,534,463) as applied to claims 16 through 20, 23 through 25, 101, 116 through 120, 123 through 125, and 129 above, and further in view of Cox (U.S. Patent No. 6,166,439). Applicants respectfully traverse this rejection, as hereinafter set forth.

Claims 21 and 22 depend from independent claim 16. As proposed to be amended herein, claim 16 defines over Lee et al., and Cox fails to cure the deficiencies of Lee. Similarly, claims 121 and 122 depend from independent claim 116. As proposed to be amended herein, claim 116 defines over Lee et al., and Cox fails to cure the deficiencies of Lee.

Therefore, claims 21, 22, 121 and 122 are allowable.

Obviousness Rejection Based on U.S. Patent No. 6,074,943 to Brennan et al. in view of U.S. Patent No. 6,277,745 B1 to Liu et al., U.S. Patent No. 6,166,439 to Cox, and further in view of U.S. Patent No. 6,046,502 to Matsuno

Claim 114 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Brennan et al. (U.S. Patent No. 6,074,943) in view of Liu et al. (U.S. Patent No. 6,277,745 B1), Cox (U.S. Patent No. 6,166,439), as applied to claims 2, 3, 100, 102 through 113, and 115 above, and further in view of Matsuno (U.S. Patent No. 6,046,502). Applicant respectfully traverses this rejection, as hereinafter set forth.

Claim 114 ultimately depends from claim 102. Matsuno fails to cure the previously noted deficiencies in Brennan et al. and Liu et al. Therefore, claim 114 is allowable as depending from claim 1.

Drawings

Applicant previously filed a Letter to the Chief Draftsman on August 4, 2000, which was received by the Office on August 4, 2000 (see attached copy of USPTO date-stamped postcard evidencing receipt of the Letter to the Chief Draftsman by the Office). The Letter to the Chief Draftsman, proposed corrections to FIGS. 3a, 3b, and 5 of the drawings. Specifically, FIGS. 3a and 3b were revised to add reference numeral 100 with appropriate lead lines; and FIG. 5 was revised to add reference numeral 62a.

The drawings have now been objected to by the Examiner for failing to mention "element 62a." This drawing objection has been overcome by the enclosed copy of the above-identified Letter to the Chief Draftsman filed on August 4, 2000, a copy of the date-stamped postcard also being included herewith to evidence receipt of same by the Office. Applicant's undersigned attorney has recolored the proposed corrections on the copies of the revised drawings to assist the Examiner. Otherwise, the paper is as previously filed. Review and approval of the proposed revisions to the drawings is respectfully requested. Applicant will file a corrected set of formal drawings upon an indication that the proposed revisions are approved.

ENTRY OF AMENDMENTS

The proposed amendments to claims 1, 12, 16, 26, 102, 116 and 126 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1 through 28 and 100 through 129 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully Submitted,

Joseph A. Walkowski
Registration Number 28,765
Attorney for Applicant
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110
Telephone: (801) 532-1922

Date: December 26, 2002

KWP/hlg:dlm
Enclosure: Version of Claims with Markings to Show Changes Made

N:\2269\3442.2\Amendment Final 2.wpd

VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

1. (Four times amended) A metallization structure for a semiconductor device, comprising:

a substrate comprising a substantially planar upper surface; and

a conductive line for transmitting a signal laterally across said substrate, said conductive line comprising:

a metal layer defining a pattern on a portion of the substrate upper surface;

a single conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said single conducting layer having substantially aligned sidewalls and said single conducting layer including an upper surface out of contact with any metal and defining an upper surface of said conductive line; and

metal spacers flanking and extending at least substantially to a [the same] height [as the] of the sidewalls of the single conducting layer and metal layer.

12. (Three times amended) The metallization structure of claim 1, further comprising a dielectric layer on the single conducting layer and having sidewalls aligned with said sidewalls of the single conducting layer, the metal spacers extending along the sidewalls of the dielectric layer.

16. (Four times amended) A metallization structure for a semiconductor device, comprising:

a substrate having a metal layer extending over said substrate, said metal layer at least underlying a conductive line, said conductive line for transmitting a signal across said substrate;

a dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said at least one sidewall of said aperture defining said conductive line;

a metal spacer abutting at least one sidewall of said at least one sidewall of the aperture and in contact with said dielectric layer, said metal spacer in contact with said underlying metal layer; and

a conductive layer in contact with said metal spacer, said conductive layer substantially filling a remaining portion of the aperture and having an upper surface substantially coincident with an upper surface of said dielectric layer.

26. (Amended) A metallization structure for a semiconductor device, comprising:

a substrate having a metal layer extending over said substrate, said metal layer at least underlying a conductive line, said conductive line for transmitting a signal across said substrate;

a dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said at least one sidewall of said aperture defining said conductive line;

a metal spacer abutting at least one sidewall of said at least one sidewall of the aperture and in contact with said dielectric layer, said metal spacer in contact with said underlying metal layer;

a conductive layer in contact with said metal spacer, said conductive layer substantially filling a remaining portion of the aperture; and

[The metallization structure of claim 16, further comprising] at least one upper metal layer on the conductive layer [and] comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN, said at least one upper metal layer being disposed within said aperture laterally adjacent said metal spacer and having an upper surface substantially coincident with an upper surface of said dielectric layer and an uppermost extent of said metal spacer.

102. (Three times amended) A structure for transmitting a signal across a semiconductor device, said structure comprising:

a substrate comprising a substantially planar upper surface; and

a conductive line extending over said upper surface and isolated therefrom by a dielectric layer at least underlying said conductive line, said conductive line comprising:

a metal layer above said dielectric layer, said metal layer defining a pattern on a portion of the substrate upper surface;

a single conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said single conducting layer having substantially aligned sidewalls, wherein an upper surface of said single conductive layer is out of contact with any metal and defines an upper surface of said conductive line; and

metal spacers flanking and extending at least substantially to a [the same] height [as the] of the sidewalls of the single conducting layer and metal layer

116. (Three time amended) A structure for transmitting a signal laterally across a substrate of a semiconductor device, said structure comprising:

a substrate having a metal layer of a conductive line disposed thereon;

a dielectric layer above said metal layer, said dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said aperture at least extending a length of said conductive line;

a metal spacer flanking at least one sidewall of said at least one sidewall of the aperture and in contact with said dielectric layer, said metal spacer in contact with said underlying metal layer; and

a conductive layer in contact with said metal spacer, said conductive layer substantially filling a remaining portion of the aperture and having an upper surface substantially coincident with an upper surface of said dielectric layer.

126. (Amended) A structure for transmitting a signal laterally across a substrate of a semiconductor device, said structure comprising:

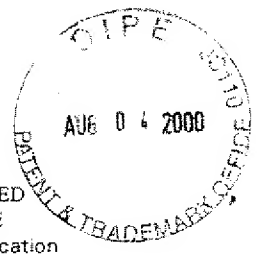
a substrate having a metal layer of a conductive line disposed thereon;

a dielectric layer above said metal layer, said dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer, said aperture at least extending a length of said conductive line;

a metal spacer flanking at least one sidewall of said at least one sidewall of the aperture and in contact with said dielectric layer, said metal spacer in contact with said underlying metal layer;

a conductive layer in contact with said metal spacer, said conductive layer substantially filling a remaining portion of the aperture; and

[The structure of claim 116, further comprising] at least one upper metal layer on the conductive layer and comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN, said at least one upper metal layer being disposed within said aperture laterally adjacent said metal spacer and having an upper surface substantially coincident with an upper surface of said dielectric layer and an uppermost extent of said metal spacer.



THE PATENT & TRADEMARK OFFICE MAILROOM DATE STAMPED HEREON IS AN ACKNOWLEDGEMENT THAT ON THIS DATE THE PATENT & TRADEMARK OFFICE RECEIVED: Utility Patent Application

Preliminary Amendment (4 pages); Letter to the Chief Draftsman (2 pages) and attached revised figures with annotations in red (3 sheets, 3 figures).

Invention: METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME
Applicant(s): Salman Akram
Filing Date: September 1, 1999
Serial No.: 09/388,031
Date Sent: August 1, 2000 via First Class Mail
Client/Matter Docket No.: 2269/3442US JAW/dlm

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Salman Akram

Serial No.: 09/388,031

Filed: September 1, 1999

For: METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME

Examiner: To be assigned

Group Art Unit: 2812

Attorney Docket No.: 3442US (96-428)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail (under 37 C.F.R. § 1.8(a)) on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, Washington, D.C. 20231.

August 1, 2000
Date of Deposit

Signature of registered practitioner or other person having reasonable basis to expect mailing to occur on date of deposit shown pursuant to 37 C.F.R. § 1.8(a)(1)(ii)

Joseph A. Walkowski
Typed/printed name of person whose signature is contained above

LETTER TO THE CHIEF DRAFTSMAN

Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicant submits herewith revised FIGS. 3a, 3b and 5 which correct errors in the drawings. Specifically, FIGS. 3a and 3b have been revised to add the reference numeral 100 with appropriate lead lines; and FIG. 5 has been revised to add the reference numeral 62a.

No new matter has been added. Approval of the proposed revisions is respectfully requested.

Respectfully submitted,

Joseph A. Walkowski
Registration No. 28,765
Attorney for Applicant
TRASK BRITT
P. O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: (801) 532-1922

Date: August 1, 2000

JAW/kf:dlm

N:\2269\3442\Letter to Chief Draftsman.wpd

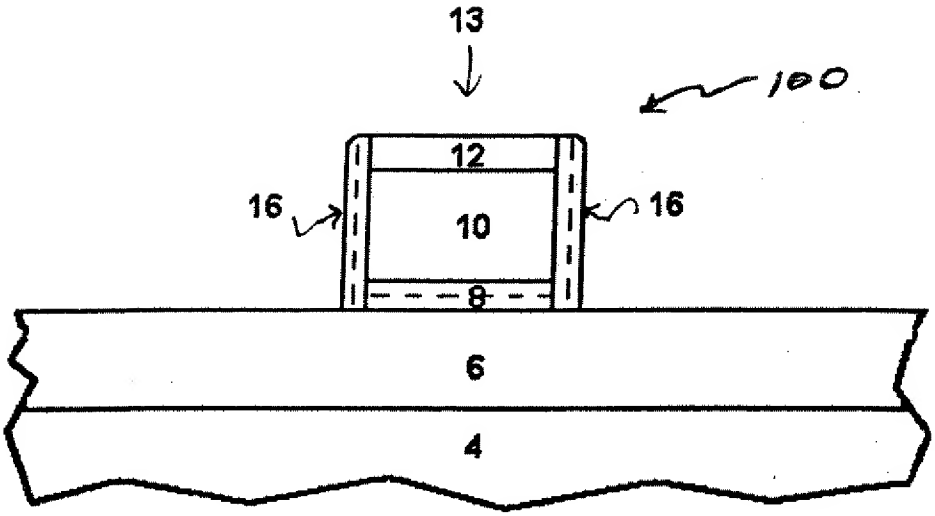


Figure 3a

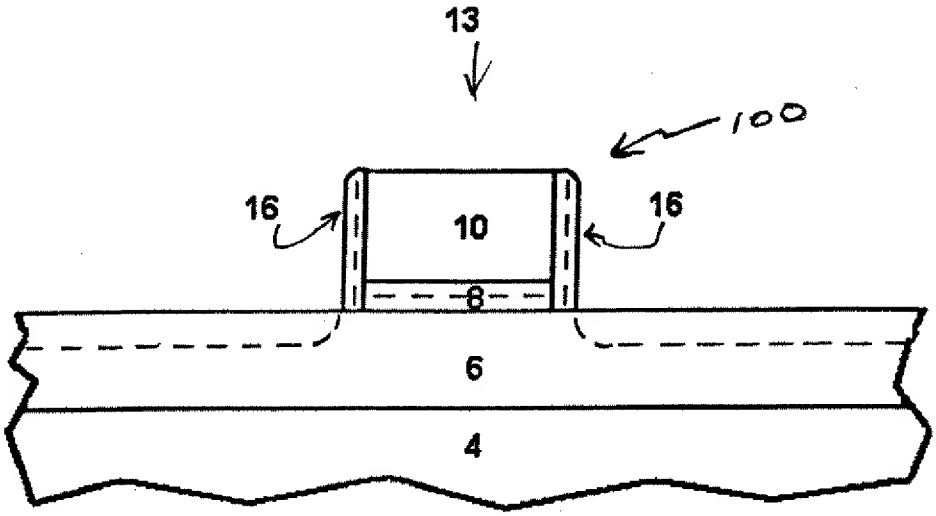


Figure 3b

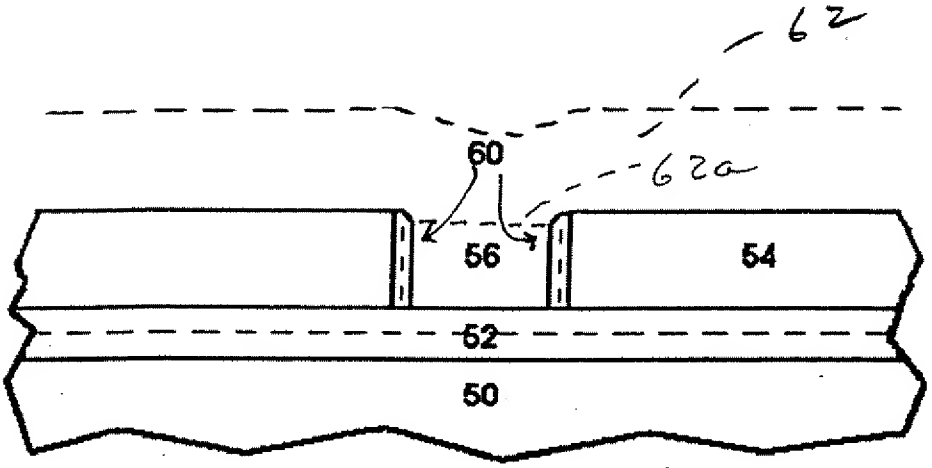


Figure 5